

ABSTRACT

A method and apparatus for testing semiconductor memory chips, such as DRAMs, having a plurality of memory cells or bits. Each memory chip has a unique identifier stored in a database. Tests are performed on the memory chips and when a memory chip fails a test, the memory chip is placed in a repair bin and a test identifier is stored in the database in association with the memory chip identifier. In order to repair the memory chip, failed tests are read out of the database and such tests are again performed on the failed memory chip in order to determine which memory cell in the memory chip is faulty. The failed memory cells are then repaired.